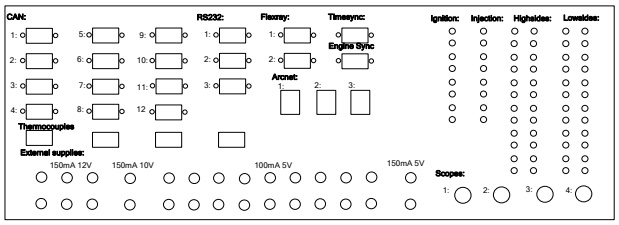
McLaren ELECTRONIC SYSTEMS

Factory HIL
vTAG-RT

Front Panel View



The Factory HIL provides a way of simulating the complete functionality of an F1 race car. I/O and simulation models are provided to drive the F1 Standard ECU components to simulate a typical run of the car i.e. engine start, pull away, and flying lap simulation including gear shifting.

The HIL can also be used for car model and ECU set-up development. The HIL provides the connectivity for the majority of the I/O of all the FIA Standard ECU components (TAG-310B, 4xHIU-3, Powerbox2006, CBT-610, PCU-6C) plus optional connection for the HSL-500 High Speed Logger.

The HIL is enclosed in a 9U rack including the PSU for the HIL and the car electronics. The units are connected via harnesses connected to the back of the rack. The PCU-6C is mounted on the front of the rack, which also provides connections for all CAN and other communication buses as well as scope outputs for the TAG-310B and Powerbox2006.

The HIL plant model runs under vTAG-RT, allowing models to be developed in Dymola or Simulink with GDE 8.1 and for ATLAS & System Monitor to be used as front ends.

Processor

- Core2 Duo 2.13GHz processor
- 2GB RAM
- 256Mb IDE flash disk

Communications

- 1 Gigabit Ethernet
- Integrated Gigabit Ethernet switch
- 6 CAN buses

I/O

- 128 x 16bit 0-5V analog output channels (expandable to 192 channels)
- 32 x 16bit analog input channels (e.g. +/-10mA Moog drive monitoring)
- 48 x digital I/O channels
- FPGA cards provide generation of crank and cam signals, and monitor TAG-310B ignition/injection timing and high/low side driver outputs. Feedback is provided via front panel LEDs and loads (10% of rated output)

Application

Full system simulation and car systems testing. The HIL is provided with a simple model that is able to drive the car around a basic circuit profile. The auto driver controls throttle, brakes and gears so that the embedded code in the TAG-310B runs as if it was on a real car.

The model is supplied as a Simulink source code so that it can be extended or replaced with teams own models.

The HIL runs vTAG-RT which provides an identical development environment to the ECU, i.e. it provides a logger which can be setup via System Monitor and monitored with ATLAS

Mounting

Harnesses are included for a TAG-310B, Powerbox2006, CBT-610, PCU-6C and 4 HIU-3s. (these units are not included). The system as a whole is a 9U rack.

25/05/10

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The Factory HIL provides the following connectivity to the FIA Standard ECU units

Unit	Unit Signal Type	vTAG-RT System Connection	Comment
TAG-310B	0-5V Analog Inputs	Direct connection to DAC channel	
	0-5V/PT1000 Analog Inputs	Direct connection to DAC, or switchable to two known resistances	Under software control the input can be switched to allow full analog control or resistances equivalent to 0°C or 190°C to be connected to the TAG-310B input
	DHE Inputs	Connection to FPGA via signal conditioning	Quadrature encoding of lay/mainshaft signals is provided
	Digital Input	Connection to FPGA via signal conditioning	
	Crank/Cam Inputs	Connection to FPGAs.	20-2 crank simulation is provided as standard
	Thermocouple Inputs	Connection via thermocouple connector on front panel	No thermocouple simulation is provided but signals can be tested via an external thermocouple (or simulator)
	Lambda Inputs	A lambda simulation circuit is provided utilising one DAC and one ADC channel for each TAG-310B lambda input	A simulation of a lambda sensor is required to driver the DAC signal appropriately.
	Lap Trigger Input	FPGA output gates a DAC generated voltage	
	Ignition Outputs	Connection to FPGA via signal conditioning	Connection can to FPGA inputs can be source from Powerbox2006 if fitted Feedback LED is provided on front panel
	Injection Outputs	Connection to FPGA via signal conditioning	Connection can to FPGA inputs can be source from Powerbox2006 if fitted Feedback LED is provided on front panel
	Moog Outputs	Direct connection to differential ADC with load resistor	
	High Side Drive Outputs	Connection to FPGA via signal conditioning	Load is 10% of rated channel load. Feedback LED is provided on front panel
	Low Side Drive Outputs	Connection to FPGA via signal conditioning	Load is 10% of rated channel load. Feedback LED is provided on front panel
	Digital Outputs	Not connected	
	Scope Outputs	Connection to ADC/FPGA and via BNC connector on front panel	
	Timesync Output	Connection to FPGA via signal conditioning	Allows time synchronisation of vTAG-RT model with TAG-310B in order to allow comparison or data recorded by both
	Sensor Supply Outputs	Connection via 4mm jacks on front panel	
	Ethernet Communications	Connction to integrated Ethernet switch via breaker driven by digital output	Allow for model based simulation of umbilical disconnection

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	CAN Communications	All TAG-310B CAN buses are connected to one vTAG-RT CAN channel and are available via the front panel, and via a breakout connector on the backplane for extension of the CAN buses	
HIU-3	Wheel Speed Inputs	Connection to FPGA via signal conditioning	
	Brake Temp/Hub Accel Inputs	Direct connection to DAC channel	
	Caliper Temp PT1000 Input	Direct connection to DAC, or switchable to two known resistances	Under software control the input can be switched to allow full analog control or resistances equivalent to 0°C or 190°C to be connected to the TAG-310B input
	Pushrod Load Inputs	Not connected	
	Brake Wear LVDT Inputs	Not connected	
PB2006	Scope Outputs	Connection to ADC/FPGA and via BNC connector on front panel	
	High Side Drive Outputs	Connection to FPGA via signal conditioning	Load is 10% of rated channel load. Feedback LED is provided on front panel
CBT-610	HDLC Comms	Connection to TAG-310B and front panel	
	CAN Comms	Connection to breakout connector on the backplane	
PCU-6C	Serial Comms	Direct connection to TAG-310B	PCU-6C can be mounted on the Factory HIL front panel

Note: The system can be used with or without a Powerbox2006 connected.

Software Included

- Simple Simulink car model (source included)
- Simulink I/O Model (source included)
- Simulink blockset including FPGA functionality to support
  - 20-2 crank/cam generation
  - Ignition/Injection pulse measurement
  - DHE PWM generation with quadrature for lay/mainshaft
  - DHE discrete tooth generation
  - Switched load state and PWM condition detection
  - Time synchronisation with TAG-310B
- Simulink CAN card drivers
- Sample front panel software written in C# (source included)
- System Monitor license
- One vTAG-RT license

Software Requirements

Development of code for the Factory HIL vTAG-RT system requires the following

- GDE V8.1
- vTAG-RT PSP (includes vTAG-RT runtime)
- Mathworks Matlab R2008a (or later) including the following toolboxes
  - Simulink
  - Real Time Workshop with RTW Embedded Coder
  - xPC Target (required to rebuild I/O model)

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